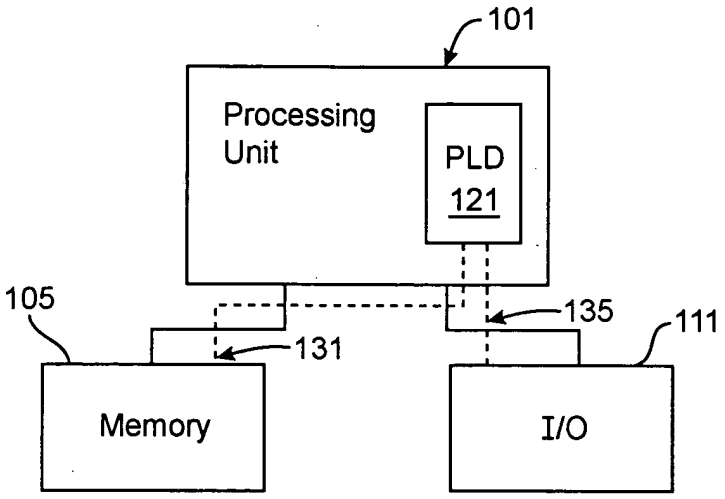
101
Processing Unit
PLD 121
105
131
135
111
Memory
I/O

FIG. 1

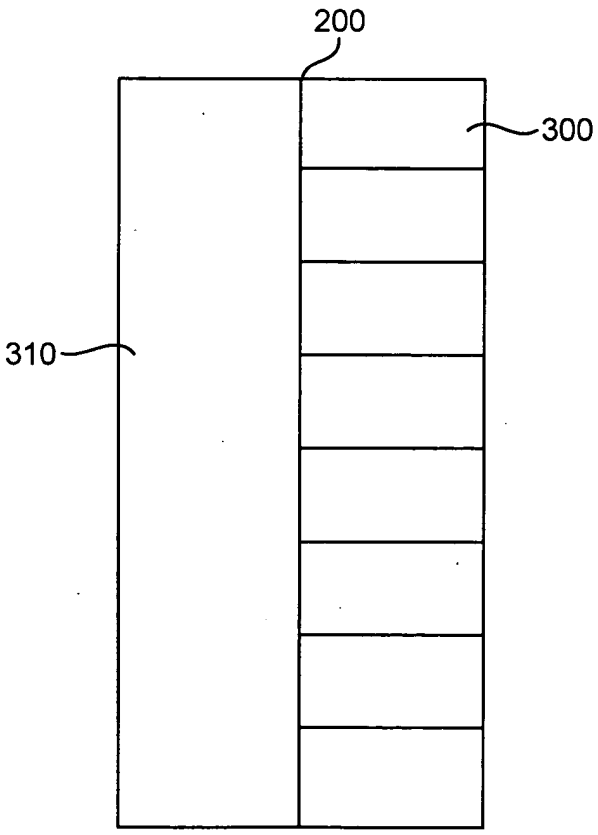
200
300
310

FIG. 3

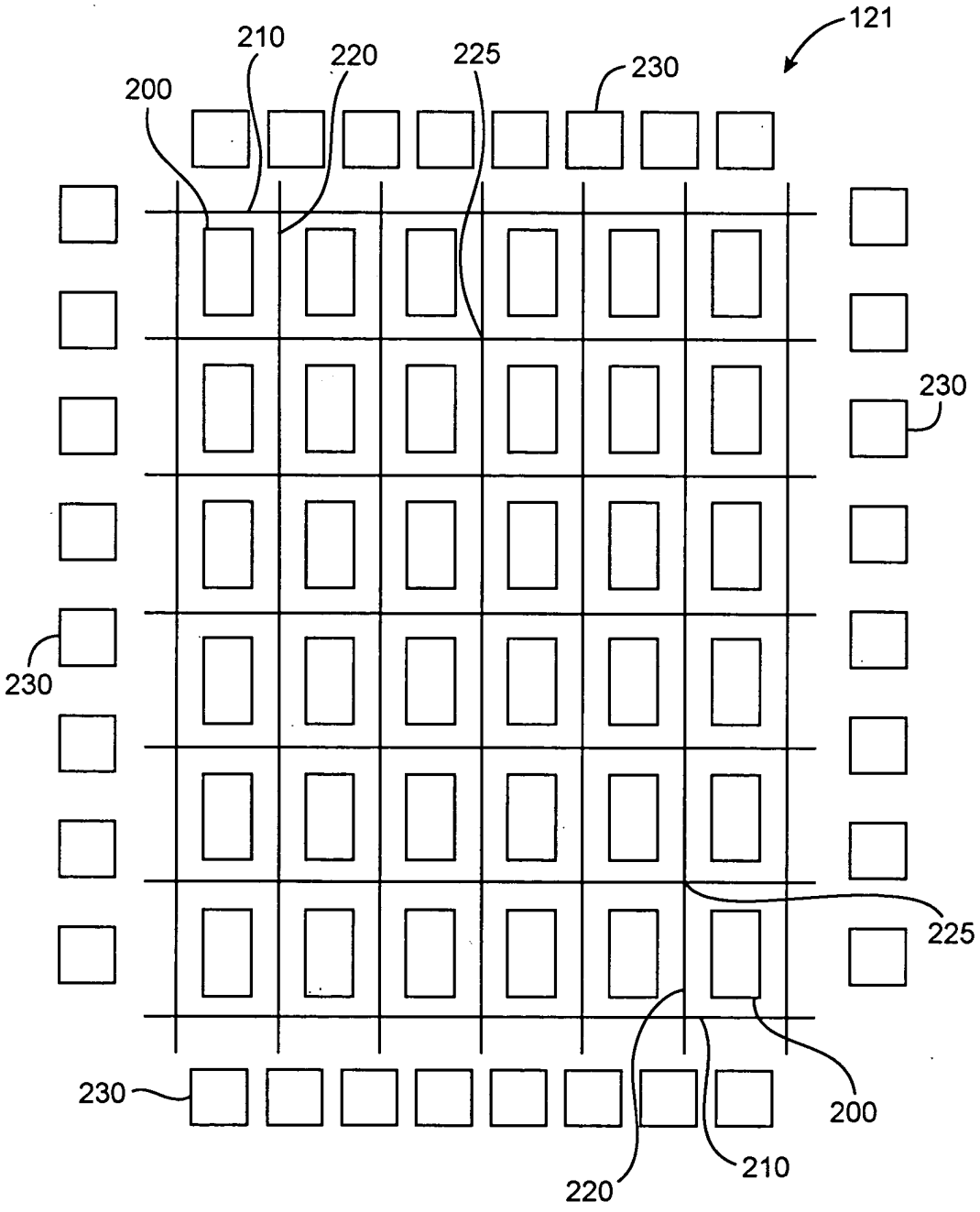

FIG. 2

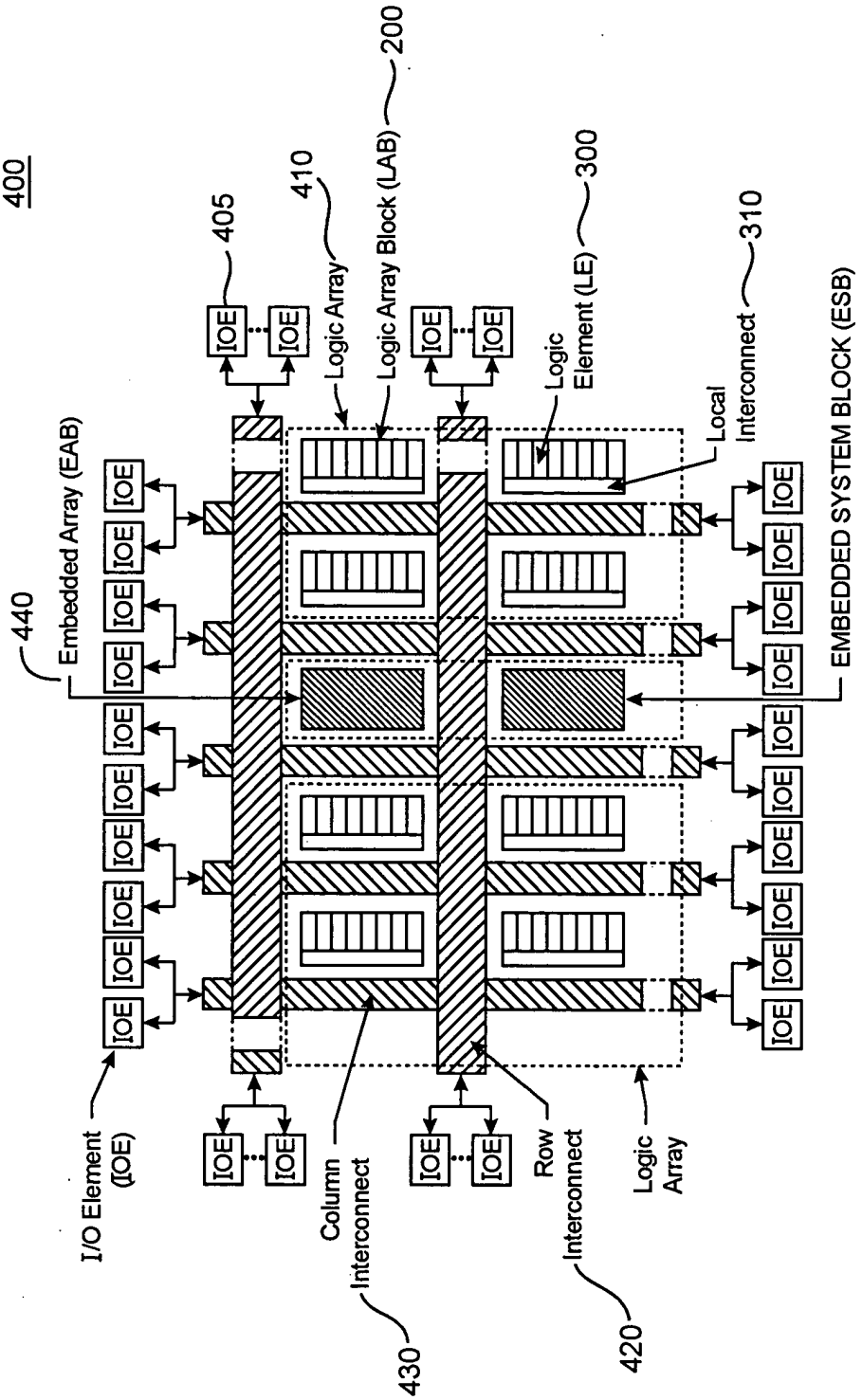
400
405
410
Logic Array
Logic Array Block (LAB)
200
300
Logic Element (LE)
310
Local Interconnect
EMBEDDED SYSTEM BLOCK (ESB)
440
Embedded Array (EAB)
IOE
I/O Element (IOE)
Column Interconnect
430
Row Interconnect
420
Logic Array

FIG. 4

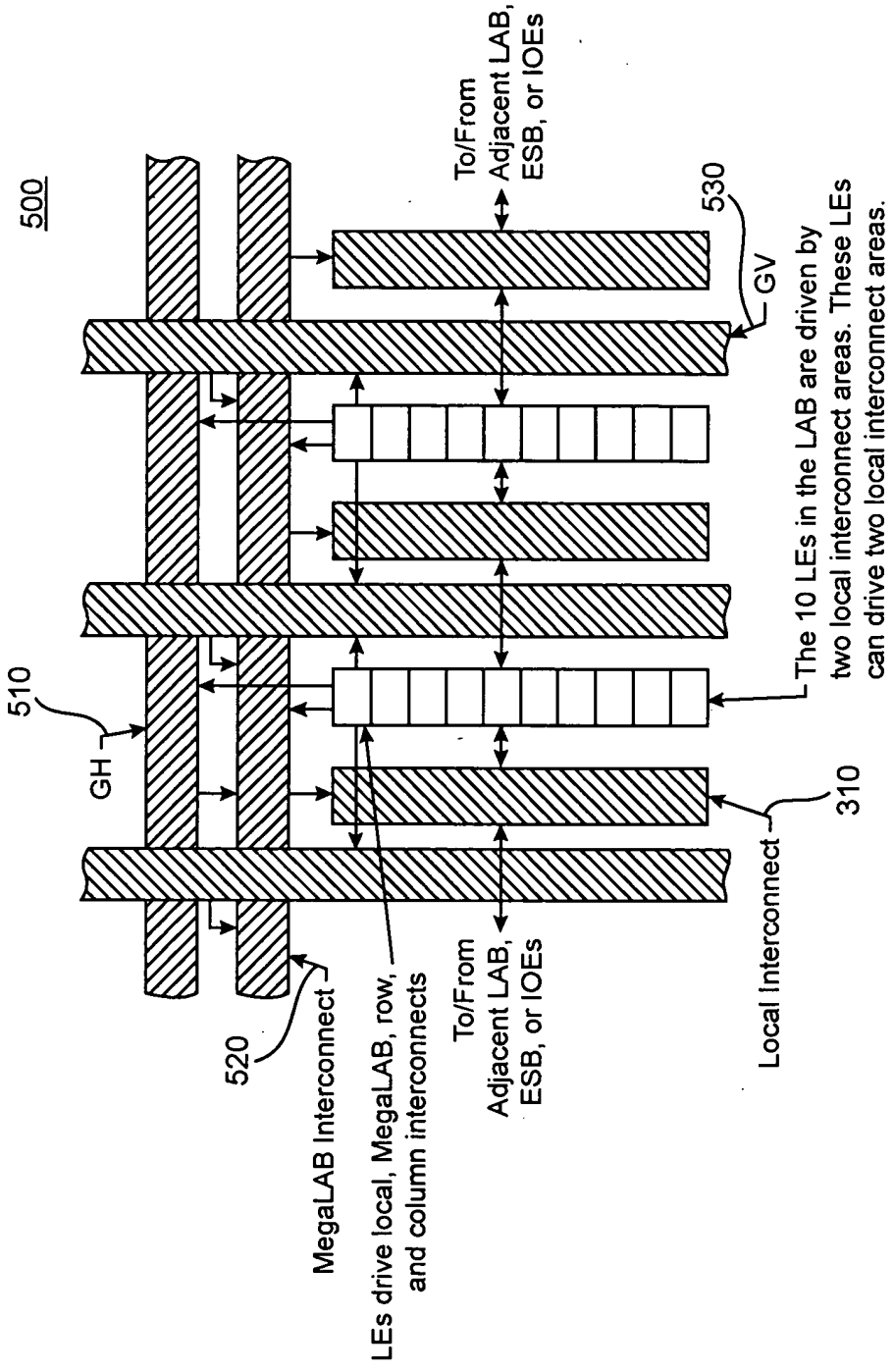
500
510
GH
520
MegaLAB Interconnect
LEs drive local, MegaLAB, row, and column interconnects
To/From Adjacent LAB, ESB, or IOEs
To/From Adjacent LAB, ESB, or IOEs
530
GV
The 10 LEs in the LAB are driven by two local interconnect areas. These LEs can drive two local interconnect areas.
310
Local Interconnect

FIG. 5

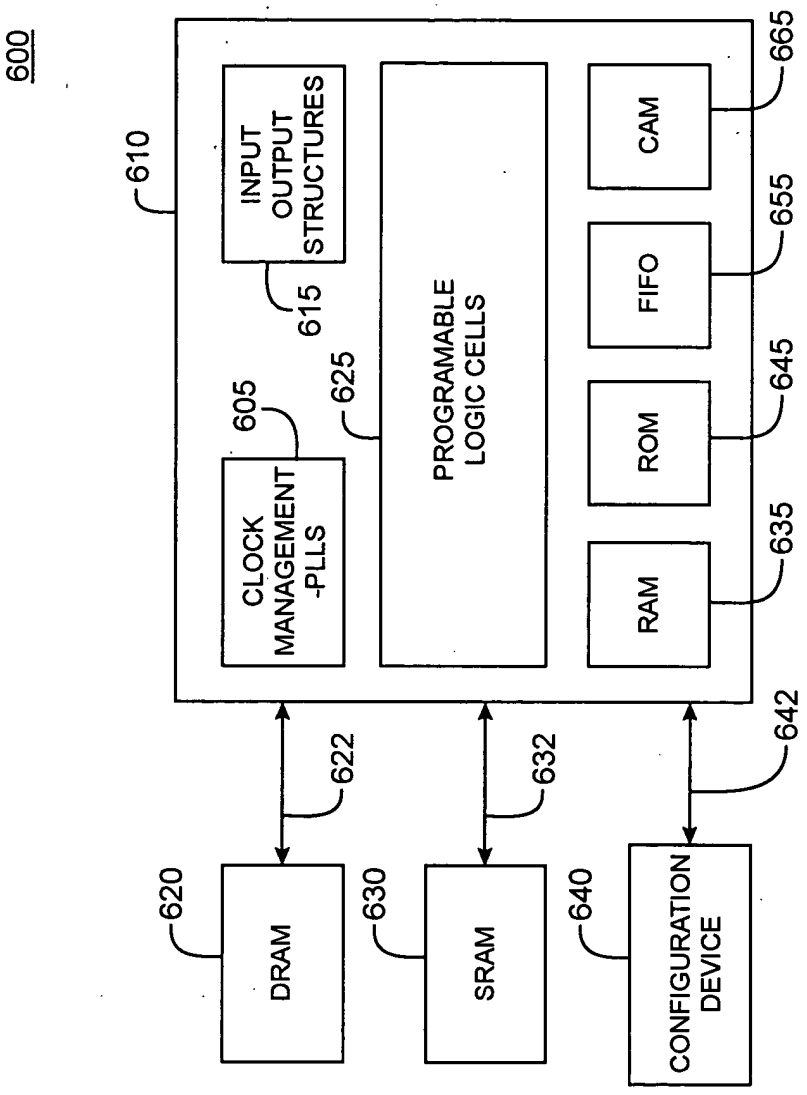
600
610
INPUT OUTPUT STRUCTURES
615
CLOCK MANAGEMENT -PLLS
605
625
PROGRAMABLE LOGIC CELLS
CAM
665
FIFO
655
ROM
645
RAM
635
642
622
632
620
DRAM
630
SRAM
640
CONFIGURATION DEVICE

FIG. 6

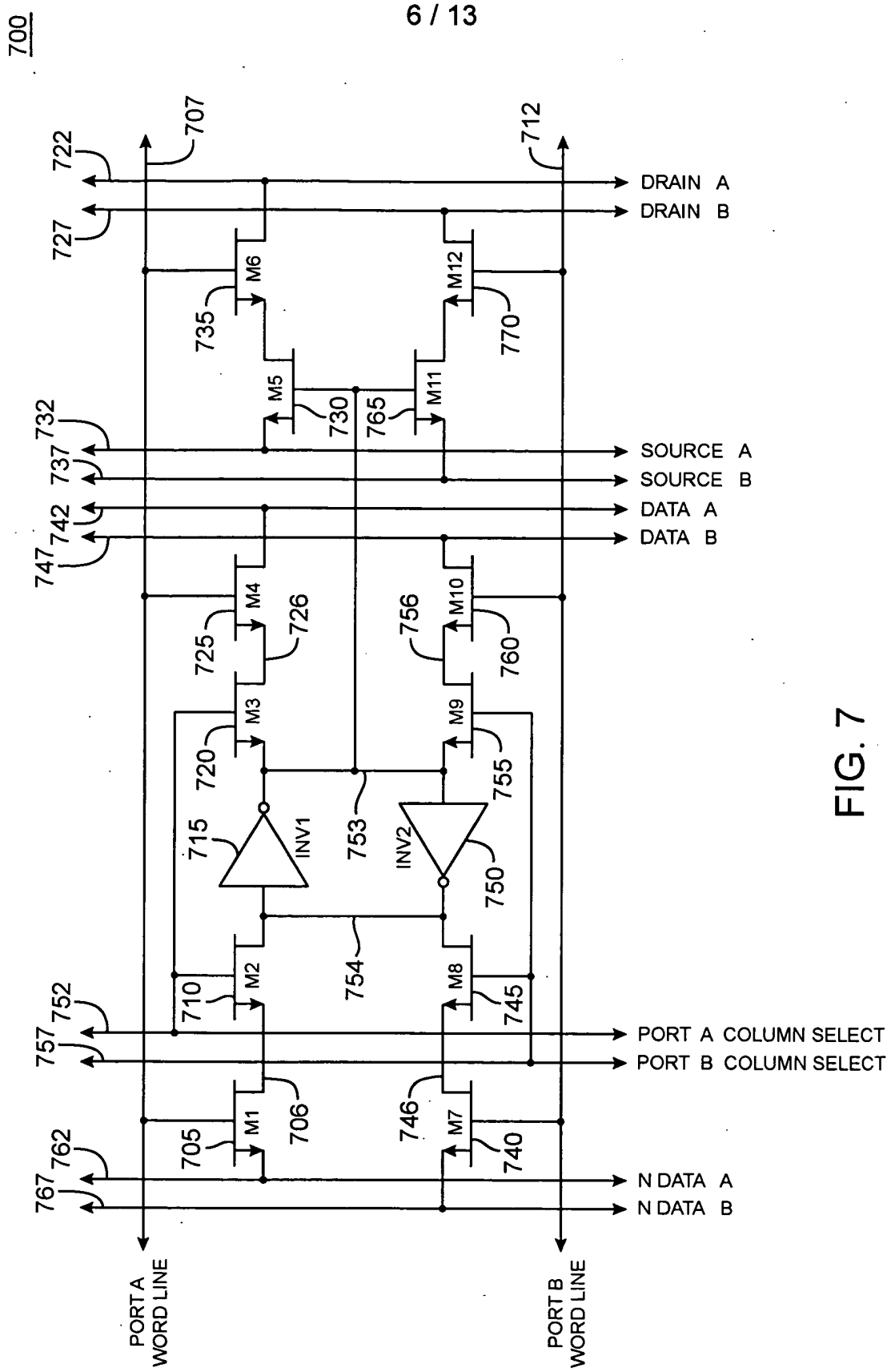
700
707
712
722
727
DRAIN A
DRAIN B
M6
M12
735
770
M5
M11
730
765
732
737
SOURCE A
SOURCE B
742
747
DATA A
DATA B
M4
M10
725
726
756
760
M3
M9
720
755
715
INV1
753
INV2
750
754
M2
M8
710
745
752
757
PORT A COLUMN SELECT
PORT B COLUMN SELECT
M1
M7
705
706
746
740
762
767
N DATA A
N DATA B
PORT A WORD LINE
PORT B WORD LINE

FIG. 7

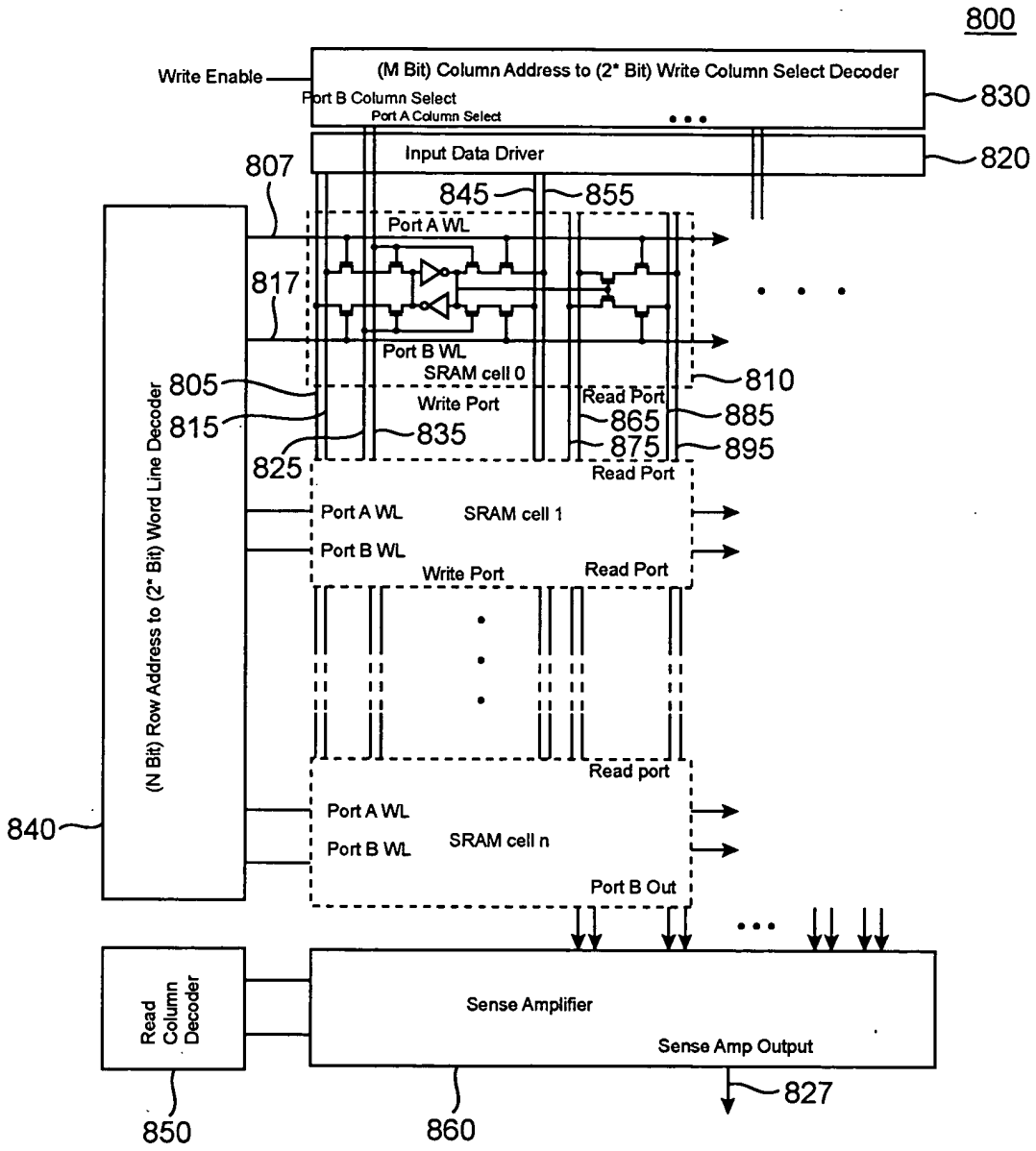
800
Write Enable
(M Bit) Column Address to (2* Bit) Write Column Select Decoder
Port B Column Select
Port A Column Select
830
Input Data Driver
820
807
845
855
Port A WL
817
Port B WL
SRAM cell 0
810
805
Write Port
Read Port
865
885
815
835
875
895
825
Read Port
Port A WL
SRAM cell 1
Port B WL
Write Port
Read Port
Read port
Port A WL
Port B WL
SRAM cell n
Port B Out
(N Bit) Row Address to (2* Bit) Word Line Decoder
840
Read Column Decoder
Sense Amplifier
Sense Amp Output
827
850
860

FIG. 8

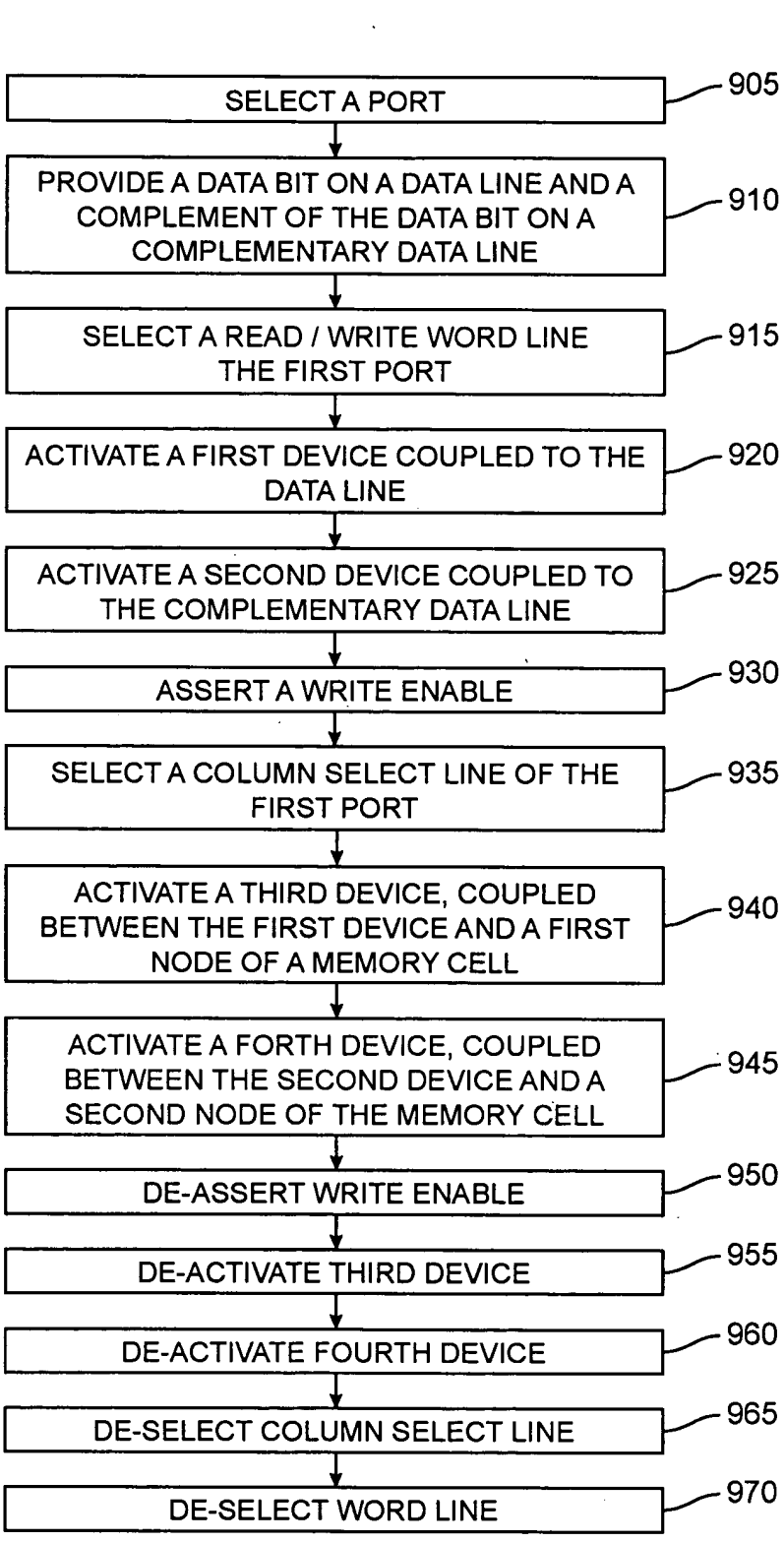
900
SELECT A PORT
905
PROVIDE A DATA BIT ON A DATA LINE AND A COMPLEMENT OF THE DATA BIT ON A COMPLEMENTARY DATA LINE
910
SELECT A READ / WRITE WORD LINE THE FIRST PORT
915
ACTIVATE A FIRST DEVICE COUPLED TO THE DATA LINE
920
ACTIVATE A SECOND DEVICE COUPLED TO THE COMPLEMENTARY DATA LINE
925
ASSERT A WRITE ENABLE
930
SELECT A COLUMN SELECT LINE OF THE FIRST PORT
935
ACTIVATE A THIRD DEVICE, COUPLED BETWEEN THE FIRST DEVICE AND A FIRST NODE OF A MEMORY CELL
940
ACTIVATE A FORTH DEVICE, COUPLED BETWEEN THE SECOND DEVICE AND A SECOND NODE OF THE MEMORY CELL
945
DE-ASSERT WRITE ENABLE
950
DE-ACTIVATE THIRD DEVICE
955
DE-ACTIVATE FOURTH DEVICE
960
DE-SELECT COLUMN SELECT LINE
965
DE-SELECT WORD LINE
970

FIG. 9

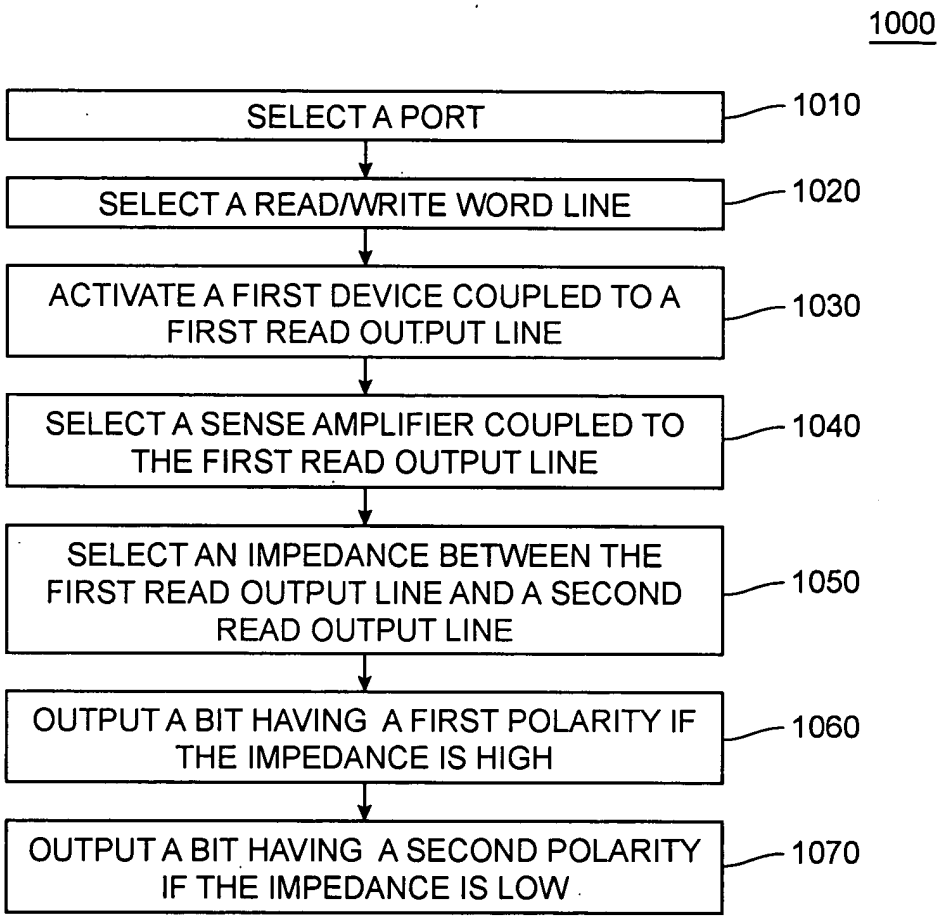
1000
SELECT A PORT
1010
SELECT A READ/WRITE WORD LINE
1020
ACTIVATE A FIRST DEVICE COUPLED TO A FIRST READ OUTPUT LINE
1030
SELECT A SENSE AMPLIFIER COUPLED TO THE FIRST READ OUTPUT LINE
1040
SELECT AN IMPEDANCE BETWEEN THE FIRST READ OUTPUT LINE AND A SECOND READ OUTPUT LINE
1050
OUTPUT A BIT HAVING A FIRST POLARITY IF THE IMPEDANCE IS HIGH
1060
OUTPUT A BIT HAVING A SECOND POLARITY IF THE IMPEDANCE IS LOW
1070

FIG. 10

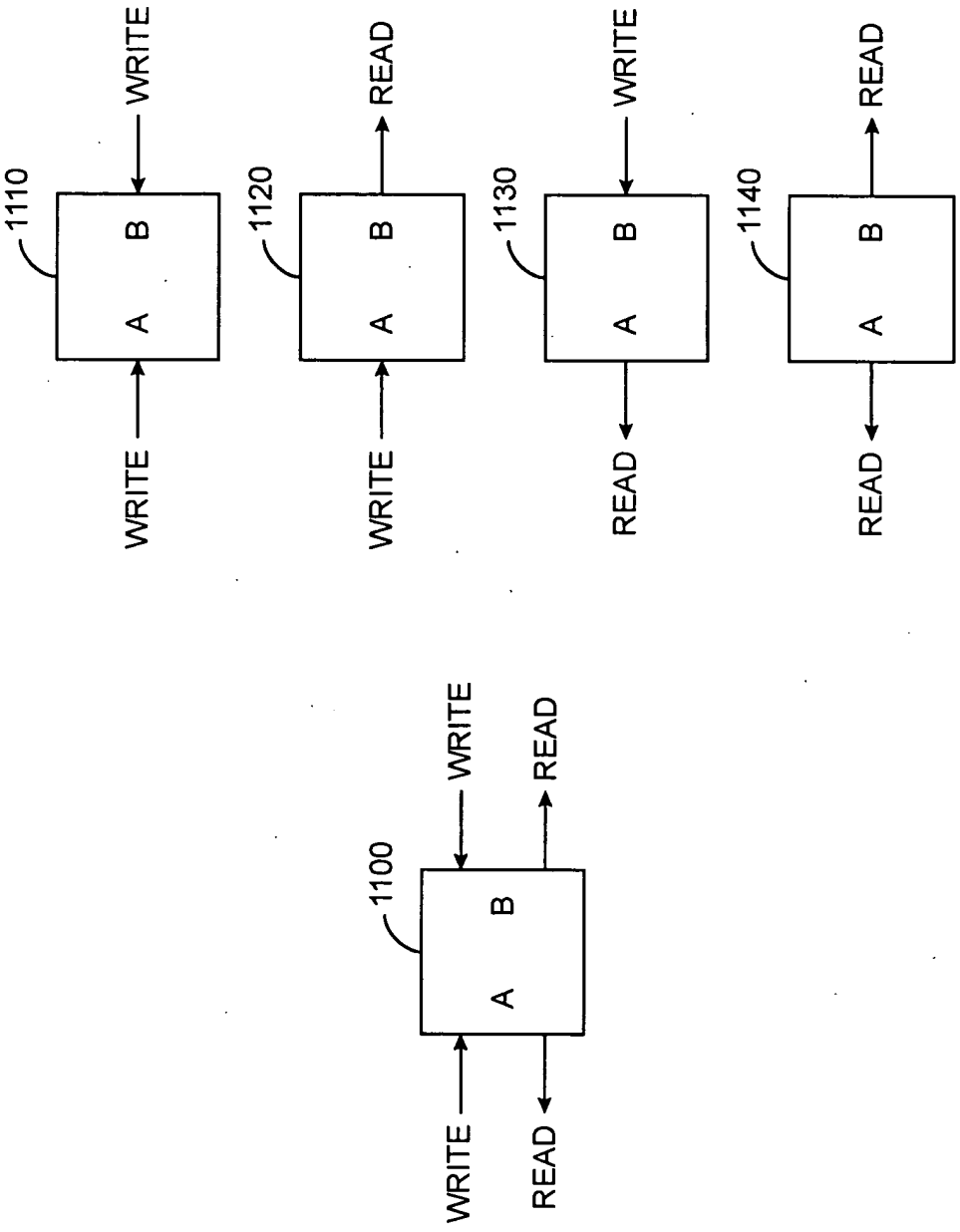
1110
WRITE
B
A
WRITE
1120
READ
B
A
WRITE
1130
WRITE
B
A
READ
1140
READ
B
A
READ
1100
WRITE
READ
B
A
WRITE
READ

FIG. 11

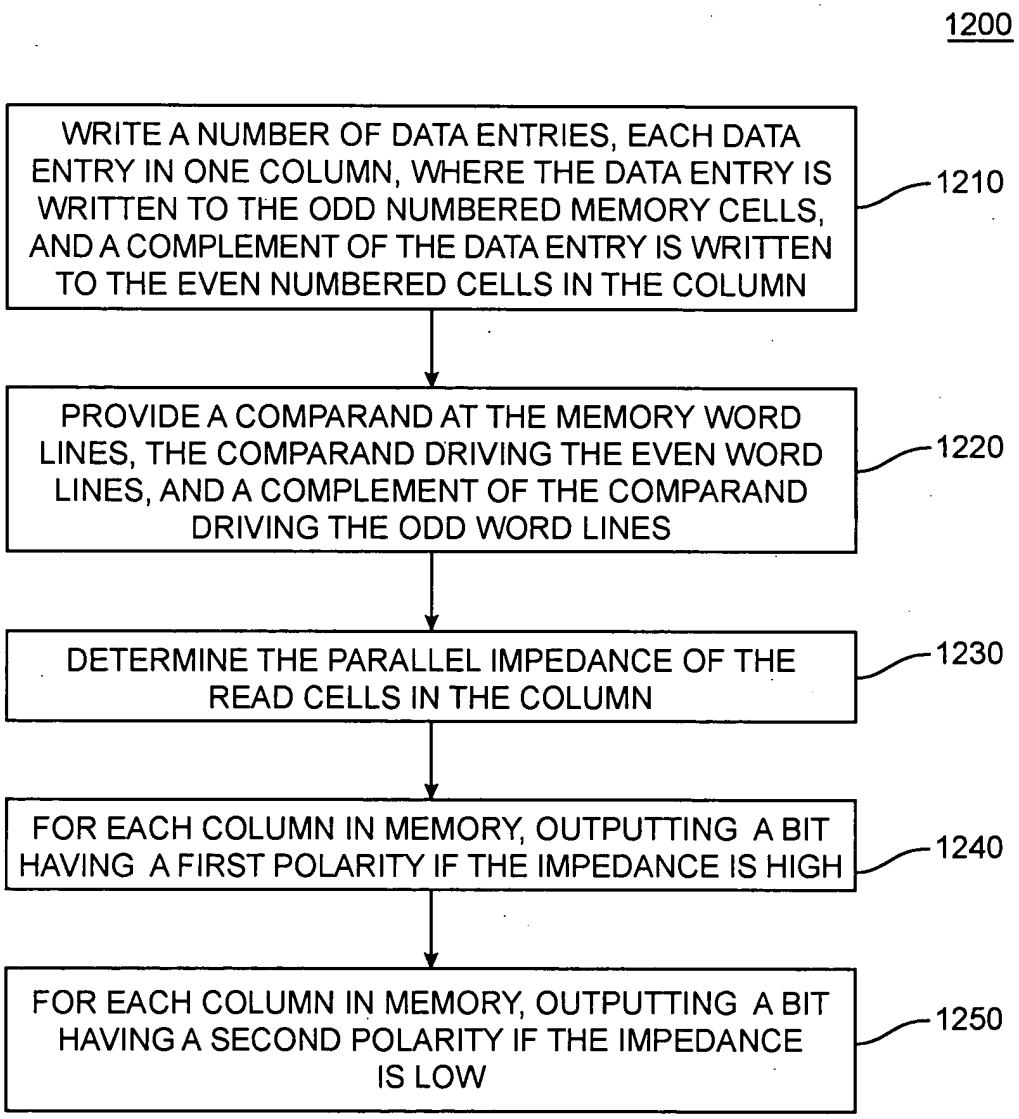
1200
WRITE A NUMBER OF DATA ENTRIES, EACH DATA ENTRY IN ONE COLUMN, WHERE THE DATA ENTRY IS WRITTEN TO THE ODD NUMBERED MEMORY CELLS, AND A COMPLEMENT OF THE DATA ENTRY IS WRITTEN TO THE EVEN NUMBERED CELLS IN THE COLUMN
1210
PROVIDE A COMPARAND AT THE MEMORY WORD LINES, THE COMPARAND DRIVING THE EVEN WORD LINES, AND A COMPLEMENT OF THE COMPARAND DRIVING THE ODD WORD LINES
1220
DETERMINE THE PARALLEL IMPEDANCE OF THE READ CELLS IN THE COLUMN
1230
FOR EACH COLUMN IN MEMORY, OUTPUTTING A BIT HAVING A FIRST POLARITY IF THE IMPEDANCE IS HIGH
1240
FOR EACH COLUMN IN MEMORY, OUTPUTTING A BIT HAVING A SECOND POLARITY IF THE IMPEDANCE IS LOW
1250

FIG. 12

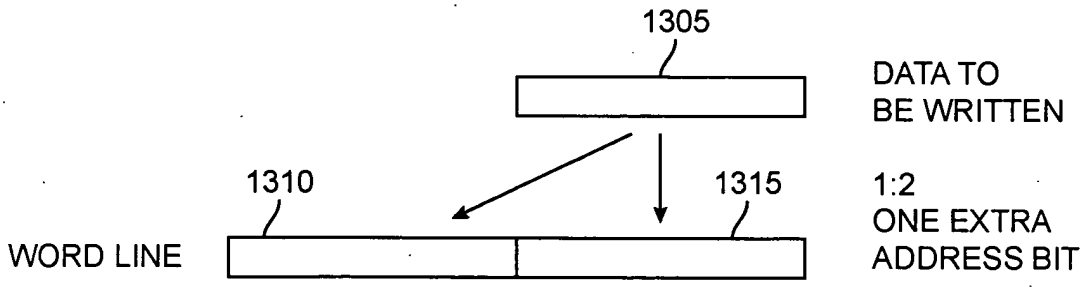

FIG. 13A

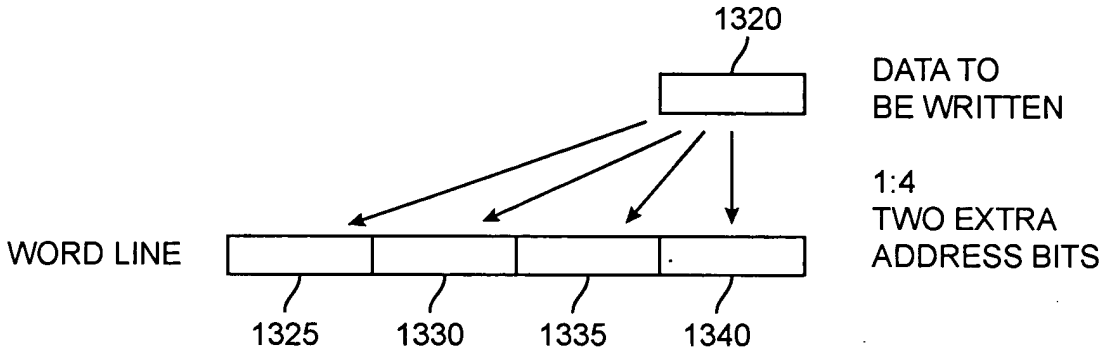

FIG. 13B

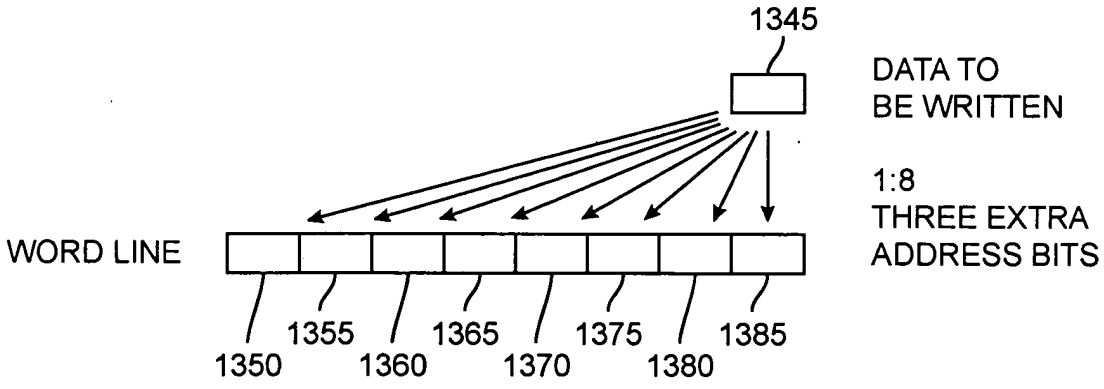

FIG. 13C

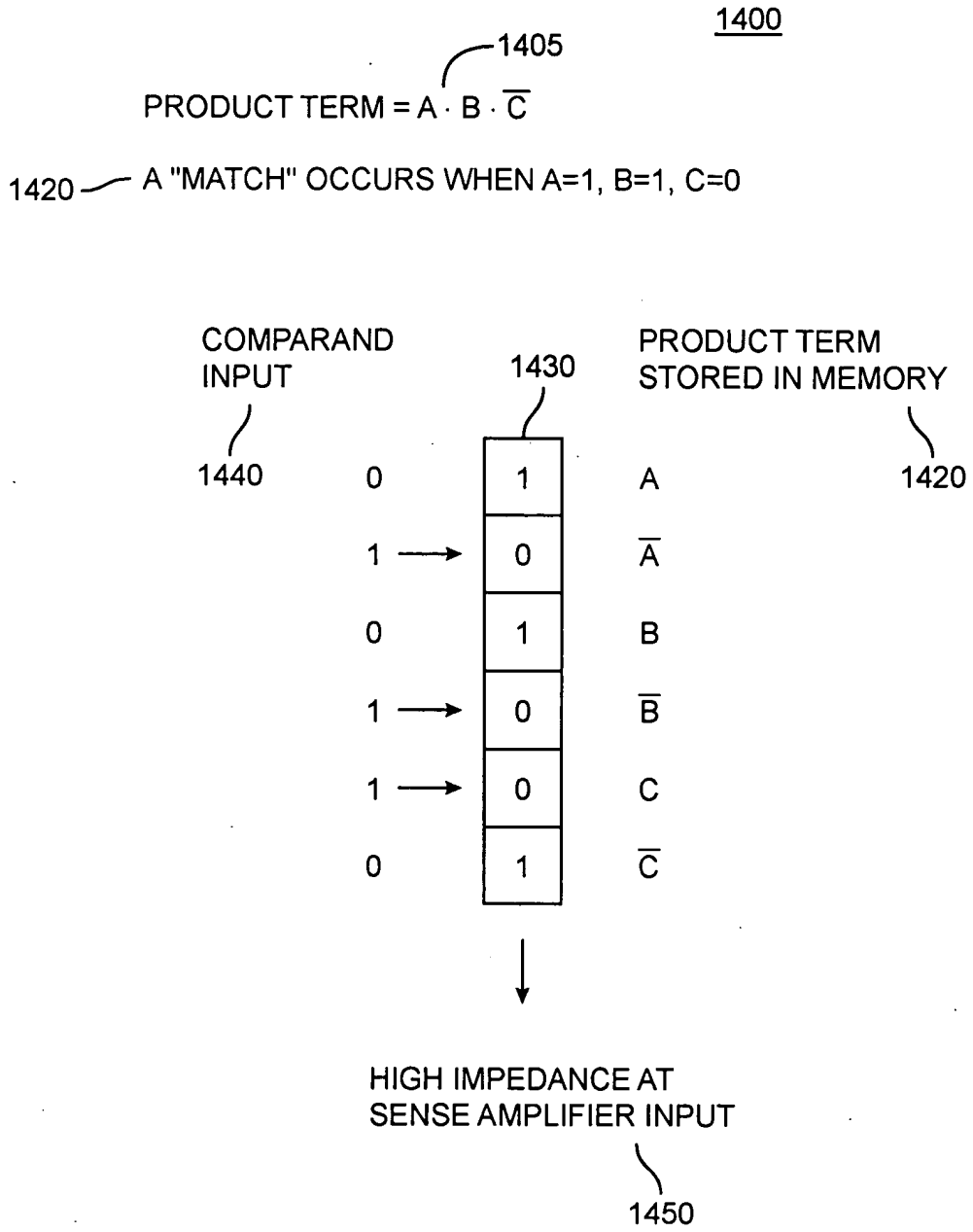
1400
1405
PRODUCT TERM = A · B · $\overline{C}$
1420
A "MATCH" OCCURS WHEN A=1, B=1, C=0
COMPARAND INPUT
1440
1430
PRODUCT TERM STORED IN MEMORY
1420
0 1 A
1 0 $\overline{A}$
0 1 B
1 0 $\overline{B}$
1 0 C
0 1 $\overline{C}$
HIGH IMPEDANCE AT SENSE AMPLIFIER INPUT
1450

FIG. 14